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# Review and comparison of methods for limiting leakage currents in single-phase transformerless PV inverter topologies

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Review article

## Abstract

Transformerless inverters are widely used in different photovoltaic nonisolated ac module applications, mainly in grid-tied photovoltaic (PV) generation systems, due to the benefits of achieving high efficiency over a wide load range, and low cost. Various transformerless inverter topologies have been proposed to meet the safety requirement of low ground leakage currents, such as specified in the VDE-4105 standard and low-output ac-current distortion. Topology modifications of transformerless full bridge inverters are designed to balance and maintain a constant common mode output voltage, thereby eliminating or reducing leakage currents.

This article reviews and compares the different methods for limiting leakage currents in known topologies of the full-bridge transformerless inverters, such as: H4, H5, H6, HERIC, and their improvements. The main topologies and strategies used to reduce the leakage current in transformerless schemes are summarized, highlighting advantages and disadvantages and establishing points of comparison with similar topologies. To compare the properties of different medium to high power inverters, PV inverter topologies were implemented using IGBTs and tested with the same components, same simulation parameters in PSPICE to evaluate their performance in terms of energy efficiency and leakage current characteristics. The detailed power stage operating principles, extended PWM modulator, and integrated universal gate driver with galvanic isolation in the transmission path of control signal for all IGBTs of the inverter, as well isolated and floating bias power supply for gate drivers are described.

## Keywords

- Differential Mode (DM)voltage
- Common Mode (CM) voltage
- grid-tied inverter
- leakage current
- parasitic capacity
- photovoltaic (PV) systems
- transformerless inverter

## Authors contributions

A – Preparation of the research project
B – Assembly of data for the research undertaken
C – Conducting of statistical analysis
D – Interpretation of results
E – Manuscript preparation
F – Literature review
G – Revising the manuscript

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# 1. Introduction

In recent decades, the grid-connected photovoltaic (PV) systems have been widely developed and applied in both commercial and residential structures. The grid-connected PV inverters are generally classified into two main groups: the galvanic isolation system and nonisolation system [1,2]. Galvanic isolation can be on the DC side in the form of a high frequency DC–DC transformer or on the grid side in the form of a low frequency but big bulky AC transformer. By using galvanic isolation, the leakage current between the PV panels and the ground can be eliminated, and the safety of the system is also increased, however overall efficiency is reduced due to power losses in additional components [2].

For many years, single-phase transformerless inverters have been developed and improved and have been successful commercial applications in the distributed PV grid-connected systems. Moreover, many advanced industrial topologies and recent innovations have been published in the last decade [3–13]. Unfortunately, galvanic connection of the grid and the DC sources in transformerless systems can introduce additional leakage currents, which depends on the value of the parasitic capacitance between the PV panels and earth and the common-mode (CM) voltage. At the same time, the CM voltage depends on the inverter topology and on the modulation strategy used. Therefore, by the improving of the modulation technique, is accomplished a decrease in the leakage current.

The grid-connected inverters, which are interfaces between the PV panels and utility grid, should satisfy the grid standards and codes, regarding with the network connection criteria, construction of the power generation system/network and system protection, as well operation of the system [14,15]. The connection standards for photovoltaic inverters establish a maximum total harmonic distortion of 5%. The standard IEC 60755 defines the detail requirements for the leakage current protection devices. According to the IEC 60755 standard, the leakage current must not exceed 300 mA, otherwise, as a safety measure, the inverter would be automatically disconnected from the power grid.

In photovoltaic applications the panels ground capacitance goes from nanofarads up to microfarads and it can vary greatly, depending on the PV panel construction and weather conditions, therefore the leakage current depends on the method of mounting the PV modules (e.g. on a foil on a metal roof) and on the weather (rain, snow) [16,17]. In many advanced industrial topologies of the low power single-phase transformerless inverters, the leakage current must not exceed 50 mA, otherwise, the inverter would be automatically disconnected from the power grid.

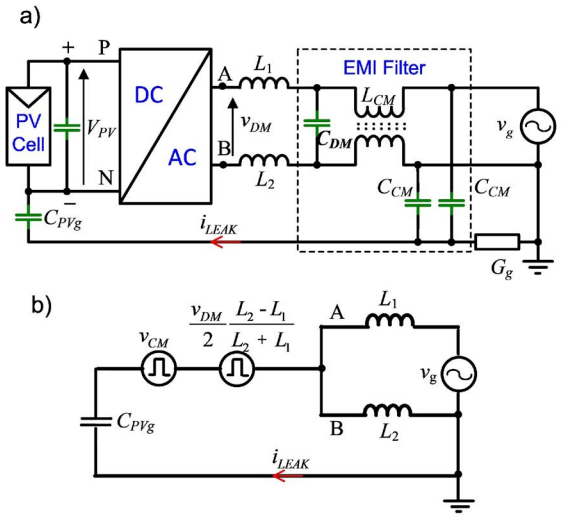


**Figure 1.** a) Typical single-phase transformerless PV inverter configuration; b) Simplified CM model

The typical single-phase voltage source inverter (VSI) is shown in Figure 1a, where:

$V_{PV}$ is the PV voltage, $C_{PVg}$ is the parasitic capacitor between the PV panels and ground, $L_1$ and $L_2$ are the two possible filter inductors, $L_{CM}$, $C_{DM}$, and $C_{CM}$, form the electromagnetic interference (EMI) filter, $v_g$ is the ac grid voltage, and $Z_{GcGd}$ is the impedance between the PV parasitic capacitor and ground, *P* and *N* are the positive and negative terminals of the PV panels.

The common-mode (CM) voltage $v_{CM}$ and differential-mode (DM) voltage $v_{DM}$ can be expressed as:

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} \tag{1}$$

$$v_{DM} = v_{AN} - v_{BN} \tag{2}$$

where $v_{AN}$ and $v_{BN}$ are the voltages of terminals A and B to terminal N.

From equations (1), (2) we get:

$$v_{AN} = v_{CM} + \frac{v_{DM}}{2} \tag{3}$$

$$v_{NB} = v_{CM} - \frac{v_{DM}}{2} \tag{4}$$

The voltages expressed by equations (3) and (4) are modeled as a voltage source in a simplified CM model as shown in Figure 1b. As we see, the DM voltage $v_{DM}$ may have some clear influence on the leakage current generation.

The equivalent CM voltage $v_{ECM}$, which is transformed from the DM voltage, is derived by:

$$v_{ECM} = v_{CM} + \frac{v_{DM}}{2}\frac{L_2 - L_1}{L_2 + L_1} \tag{5}$$

If the filter inductors are identical ($L_1 = L_2$) then:

$$v_{ECM} = v_{CM} = \frac{v_{AN} + v_{BN}}{2} \quad \text{for } L_1 = L_2 \tag{6}$$

Many solutions have been proposed to realize CM voltage constant in the full-bridge transformerless inverters [3–13,18,19]. A half-bridge inverter is the typical solution to keep the CM voltage constant [4]. However, a half-bridge inverter requires double the DC input voltage of the full bridge inverter, which requires a DC-DC converter with an extremely high conversion ratio. As a result, this can lead to a huge decrease in system efficiency. The traditional method is to use a topology-modified full bridge inverter using three-level sinusoidal pulse width modulation (SPWM). It is desirable that the CM voltage of this inverter be kept constant in all operating modes. As a result, it features excellent leakage currents characteristic. However, in some designs of full-bridge transformerless inverters, the CM voltage are not kept constant in all operating modes, which leads to high leakage currents [4,5,20]. Depending on the topology and the switching strategy, the leakage current causes increase conducted and radiated EMI, grid current distortion and additional losses in the system. Amplitude and spectrum of leakage current depends on the converter topology, on the switching strategy and on the resonant circuit formed by the parasitic capacitance to the ground, the converter, the AC filter and the grid. The grid-connected PV systems, especially the low-power single-phase systems (up to 3,68 kW), should be designed to provide high efficiency, small size, light weight and low cost.

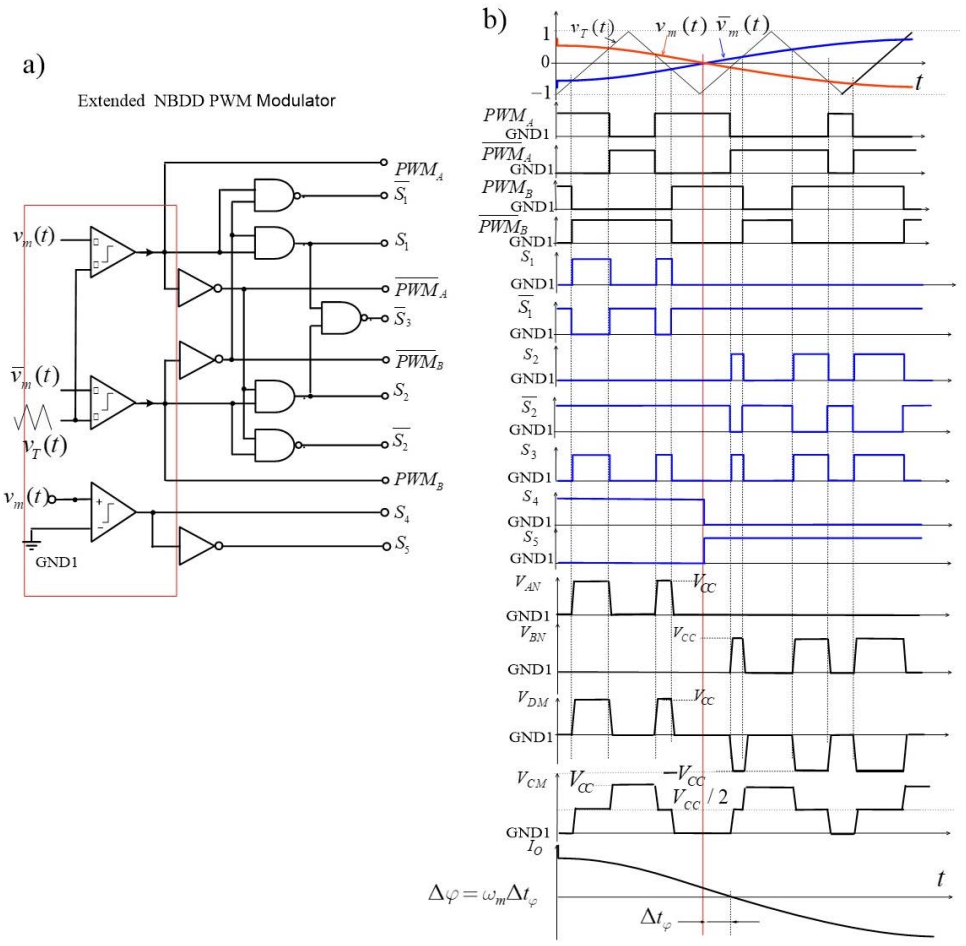


**Figure 2.** Extended NBDD PWM modulator: a) Block diagram; b) Time-domain waveforms of the generated control signals and the inverter output voltages

This paper is organized as follows. Section 2 describes the concept of an extended PWM modulators, based on the Natural sampling-BD-Double sided PWM (NBDD PWM) or Phase Shifted Carrier PWM (PSC PWM) modulation scheme, which generate signals needed to control all transistor switches of any full-bridge transformerless inverters. In this Section also an application of integrated gate driver with galvanic isolation in the transmission path of the control signal for each transistor of the inverter, as well isolated and floating bias power supply for gate driver is presented. In Section 3, the operation modes and characteristics of the known topologies of the full-bridge transformerless inverters: H4, H5, H6, HERIC, hybrid bridge, and their improvements are presented and compared. All PV inverter topologies were implemented using IGBTs and tested with the same components, same simulation parameters in PSPICE to evaluate their performance in terms of energy efficiency and leakage current characteristics. Conclusions are given in Section 4.

## 2. IGBTs control in single-phase transformerless full-bridge inverters

The transistor switches of the transformerless full bridge inverters can be controlled by PWM signals generated by an extended PWM modulator based on the NBDD PWM or PSC PWM modulation scheme.

The block diagram of the extended NBDD PWM modulator is shown in Figure 2a, and the time-domain waveforms of the generated control signals, as well the inverter output voltages are shown in Figure 2b. The designations of the inverter output voltages are the same as in Figure 1a.

NBDD PWM modulation, which is equivalent to three-level version of PSCPWM) is the best in terms of the DM output and has by far the most attractive spectral characteristic, which contains much less unwanted spectral components than all other PWM methods [21,22].

The DM and CM outputs of the NBDD modulation can be expressed after some conversion by the Double Fourier Series (DFS) expressions (eq. 7, 8) [21,22].

Equation (1) shows, that effective sampling frequency of the DM output signal is doubled without increasing the transition frequency on the output, and all harmonics around odd multiples of the switching frequency are eliminated. However CM output (eq. 2) reveals some drawback, as the frequency spectrum of the NBDD output contains the odd harmonics of the switching frequency, and their even intermodulation (IM) components. The CM output components are present at full scale even at very low level of modulating signal, which leads to high unacceptable leakage current.

$$F_{NBDD}^{DM}(t) = M\cos(\omega_m t) - \\ -4\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\left\{\frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi}\sin\left(\frac{(m+n)\pi}{2}\right)\sin\left(\frac{n\pi}{2}\right)\sin\left[m\Omega_c + n\omega_m)t - \frac{n\pi}{2}\right]\right\} = \\ = M\cos(\omega_m t) + \\ +4\sum_{m=1}^{\infty}\sum_{n=0}^{\pm\infty}\left\{\frac{J_n\left(\frac{2m\pi M}{2}\right)}{2m\pi}\sin\left(\frac{\left[2m+(2n+1)\right]\pi}{2}\right)\sin\left[\{2m\Omega_c + (2n+1)\omega_m\}t + \frac{\pi}{2}\right]\right\} \tag{7}$$

$$F_{NBDD}^{CM}(t) = 2\sum_{m=1}^{\infty}\frac{J_0\left(\frac{m\pi M}{2}\right)}{\frac{m\pi}{2}}\sin\left(\frac{m\pi}{2}\right)\cos(m\Omega_c t) + \\ +2\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\left\{\frac{J_n\left(\frac{m\pi M}{2}\right)}{\frac{m\pi}{2}}\sin\left(\frac{(m+n)\pi}{2}\right)(1+\cos n\pi)\cos\left[(m\Omega_c + n\omega_m)t\right]\right\} \tag{8}$$

where:
$\Omega_c = 2\pi F_c$ – switching angle frequency; $\omega_m = 2\pi f_m$ – angle frequency; $M$ – modulation index, $M \in [0;1]$; $J_n$ – Bessel function of $n$-th order

The output LC low-pass filter coupling the inverter output to the grid in order to suppress unwanted components of the frequency spectrum of the PWM output voltage, limit the magnitude of the output ripple current, as well as reduce the EMI, causes the load current to be out of phase with the modulating signal (with the grid voltage), As we can see in Figure 2b, the IO load current is delayed in phase with respect to the modulating signal by the phase angle: $D_j = w_m D t_j$, hence the power factor is slightly less than 1 (depending on the filter parameters).

The block diagram of the extended PSC PWM modulator is shown in Figure 3a, and the time-domain waveforms of the generated control signals as well the inverter output voltages are shown in Figure 3b.

The DM and CM outputs of the PSC PWM modulation can be expressed after some conversion by the following Double Fourier Series (DFS) expressions (eq. 9, 10) [21, 22].

$$F_{FSC}^{CM}(t) = \frac{1}{2} \tag{9}$$

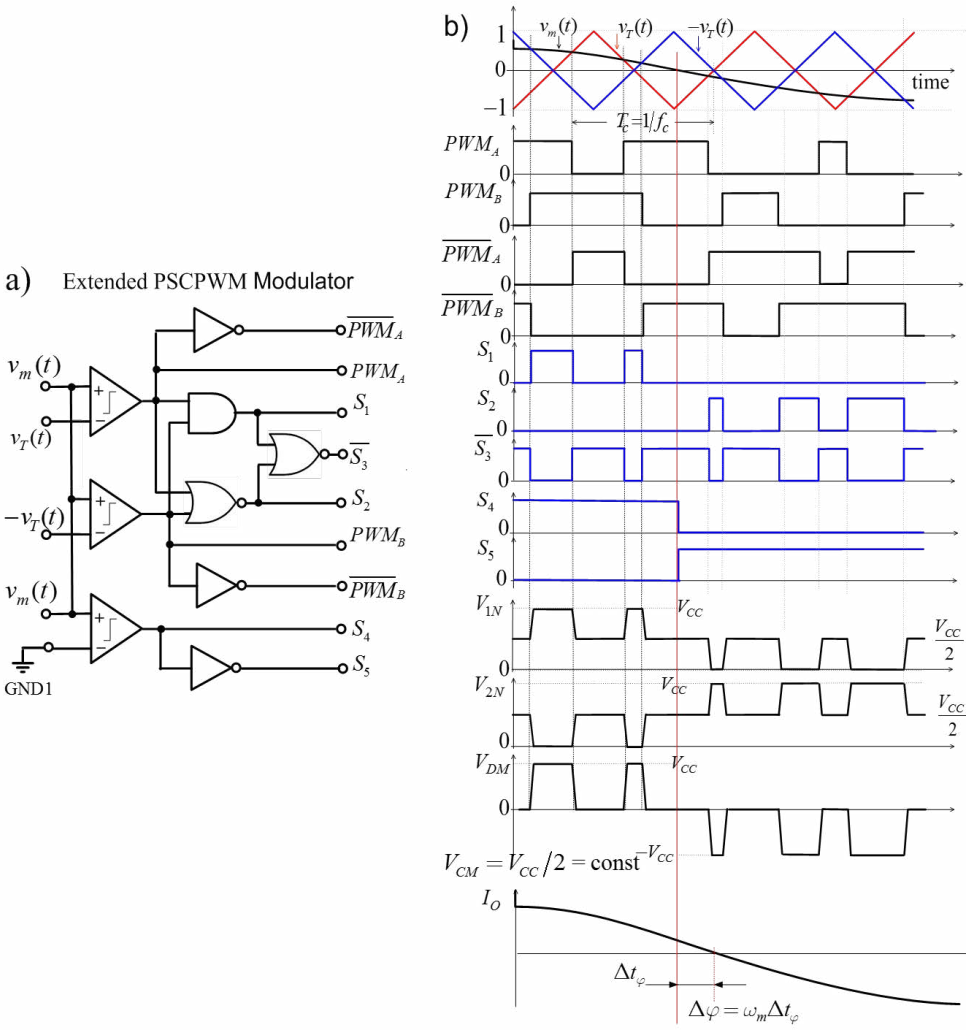


**Figure 3.** Extended PSC PWM modulator: a) Block diagram; b) Time-domain waveforms of the generated control signals and the inverter output voltages

$$F_{FSC}^{DM}(t) = M\cos(\omega_m t) + \\ + 2\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\left\{\frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi}\sin\left(\frac{(m+n)\pi}{2}\right)\left[1-\cos(n\pi)\right]\sin\left[m\,\Omega_c + n\,\omega_m)t\right]\right\} = \\ = M\cos(\omega_m t) + \\ + 4\sum_{m=1}^{\infty}\sum_{n=0}^{\pm\infty}\left\{\frac{J_n\left(\frac{2m\pi M}{2}\right)}{2m\pi}\sin\left(\frac{\left[2m+(2n+1)\right]\pi}{2}\right)\sin\left[\{2m\,\Omega_c + (2n+1)\omega_m\}t\right]\right\} \tag{10}$$

Comparing equations (7, 8) with the corresponding (9, 10) , as well Figure 2b with Figure 3b, we can see that the DM output of the Class-BD amplifier with the PSC PWM modulation is identical to that one for the optimal NBDD PWM, however PSC PWM keeps the CM output constant.

As with NBDD PWM modulation, also with PSC PWM modulation, the IO load current is delayed in phase with respect to the modulating signal by the phase angle: $D_j = w_m D t_j$, hence the power factor is slightly less than 1.

Different topology modifications of transformerless full bridge inverters form new current paths to balance and maintain constant CM output voltage, thereby eliminating or reducing leakage currents and increasing efficiency. Another solution to minimize the leakage current is an isolation of two system sources (PV, grid) during the zero-state by modifying the PWM to keep the CM voltage constant. Extended PWM modulators based on the NBDD PWM modulation scheme (Figure 2) or PSC PWM one (Figure 3) are equivalent to each other and can alternatively be used to generate all the necessary PWM control signals for various topology modifications of the transformerless full-bridge inverters.

Figure 4a shows an application of integrated gate driver with galvanic isolation in the transmission path of the control signal for each transistor of the inverter, as well isolated and floating bias power supply for gate driver, while Figure 4b shows its general block diagram with input and output voltages and signals.

The integrated gate control system shown in Figure 4 was used in this paper to control any transistor switch in each transformerless full bridge inverter, both in simulation tests in the PSPICE program and in experimental tests.

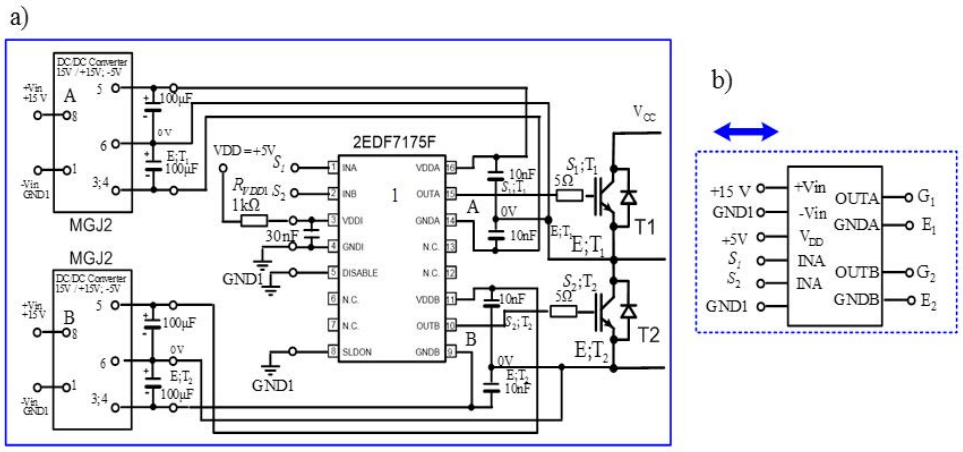


**Figure 4.** Application of integrated gate driver with galvanic isolation and floating bias power supply: a) System block diagram for two channels; b) General block diagram with input and output voltages and signals

# 3. Review and comparison of single-phase transformerless full bridge inverter topologies in terms of leakage currents

As mentioned before, due to the non-galvanic isolation configuration, the ground leakage current would appear through the PV parasitic capacitance into the ground, which induces the physical danger and serious EMI problems and needs to be eliminated or reduced to a certain level. To eliminate the leakage current, CM voltage must be kept constant for all switching states. In this section, the generation mechanism and suppression principle for the leakage current in the single-phase transformerless PV symmetrical inductor-based inverters ($L_1 = L_2$) are briefly analysed to compare the properties of different inverters.

The tested inverters were implemented on fast IGBTs of IKW50N60H3_L1 type I, Schottky diodes STPSC20065D, at the DC power supply on the primary-side of the PV system of $V_{CC} = V_{PV} = 400$V. The $f_m$ frequency of the reference signal equals to the grid frequency $f_g = 50$ Hz, while the switching frequency $Fc = 20$ kHz for the H4 inverter or $F_c = 40$ kHz for the other inverters.

To control IGBT transistors, fast dual-channel isolated MOSFET gate-driver 2EDF7175 ICs were used. These gate drivers provide functional input-to-output isolation using coreless transformer technology. The input side of each gate driver is powered by the same power supply as the PWM controllers ($V_{DD} = 5$V). The output-side gate driver voltages $V_{DDA}$ and $V_{DDB}$ ($V_{DDA} = V_{DDB} = 12$V, +5V) are generated by separate isolated auxiliary supplies, as it is shown in Figure 4. Adjusting the amplitude of the reference signal $V_g = V_m$ controls the modulation index $M$ and changes the RMS of the grid voltage $V_g$ At $V_{PV} = 400$V and $M = 0.8$, we receive maximum deviation from the rated value: RMS $V_g = 253$V.

The compared inverters have the same circuit parameters: Rate power $V_g = 253$V Input Capacitance $C_{dd} = 2$mF, Filter inductor $L_1 = L_2 = 2$mH, Filter Capacitor $C_O = 0.47$µF, PV parasitic capacitances $C_{PVg} = 0.2$µF.

Cadence OrCAD and Allegro 17.4-2019 simulation software by Cadence Design Systems, Inc. was used to test the operation of the inverter systems. It uses component models in the form of a textual description of a circuit component used by the simulator to mathematically predict its behavior under various conditions. The key element of the H-bridge here is an IGBT, and the model used in the simulation is an IGBT of the IKW50N60H3_L1 type. The model simulates the behavior of this transistor at high voltages $V_{CE} = 600$V and collector current $I_C = 50$A at the room temperature. The maximum voltage between the gate and the emitter is $V_{GE} = 20$V. The transistor model, carrying PWM signals, delays them from about 20 ns to about 230 ns. Rise and fall times are tens of nanoseconds. The simulated dissipation power of this IGBT power transistor is 330W. To drive the power transistors, a model of a fast, two-channel, isolated IGBT gate driver model was used: 2EDF7175F. It is powered by low voltages −5V and +12V and controls the operation of one H-half-bridge of the H-bridge configuration . Typical propagation times are from 30ns to 45ns. The models are provided by Infineon and fully reflect all specifications and performance characteristics of the semiconductor products to which the model applies.

Generally, there are four operating modes in any transformerless full bridge inverter:

1. Mode 1: the positive half-period in the active state.
2. Mode 2: the positive half-period in the freewheeling (Zero) state.
3. Mode 3: the negative half-period in the active state.
4. Mode 4: the negative half-period in the freewheeling (Zero) state.

In many works [ex. 4,5,7,8,23], the analysis of transformerless full bridge inverters is presented for the specific case where the power factor equals 1, which means that the grid current is in phase with the sinusoidal modulating signal (at grid frequency) used in the modulator to generate PWM control signals. In this case, in mode 2, the transistor switch is turned ON during the positive half cycle of the modulating signal, while in mode 4, the transistor switch is turned ON. during the negative half-period of the modulating signal ($S_4$, $S_5$ signals are generated in the modulators shown in Figures 2–3). The output LC low-pass filter coupling the inverter output to the grid causes that the $I_O$ load current is delayed in phase with respect to the modulating signal by the phase angle: $D_j = w_m D t_j$, hence the power factor is slightly less than 1. In the time interval $t_1$, in modes 2 and 4, the transistor switches are turned off. which leads to a large deformation of the $V_{DM}$ differential PWM output voltage and unacceptable distortions of the $I_O$ load current.

To eliminate this undesirable effect, the control signals in modes 2 and 4 must be in phase with the grid current and the capability of injecting or absorbing reactive power must be provided. This can be achieved very simply by replacing the signals $S_4$ and $S_5$ with $\bar{S}_2$ and $\bar{S}_1$ respectively (see Figures 2b and 3b).

## 3.1. H4 full bridge inverter

Figure 5 presents the topology of the simplest H4 full bridge inverter, which is controlled by the unipolar $PWM_A$ and $PWM_B$ signals (and their negations), generated by the extended NBDD modulator, shown in Figure 2a. The idealized voltage waveforms at the DM and CM outputs of the inverter are similar to those in Figure 2b. NBDD modulator compares the sinusoidal voltage and its inverse to the triangle carrier and switches each side of the bridge independently, thereby creating a three-level, DM output voltage, and there are four modes of operation.

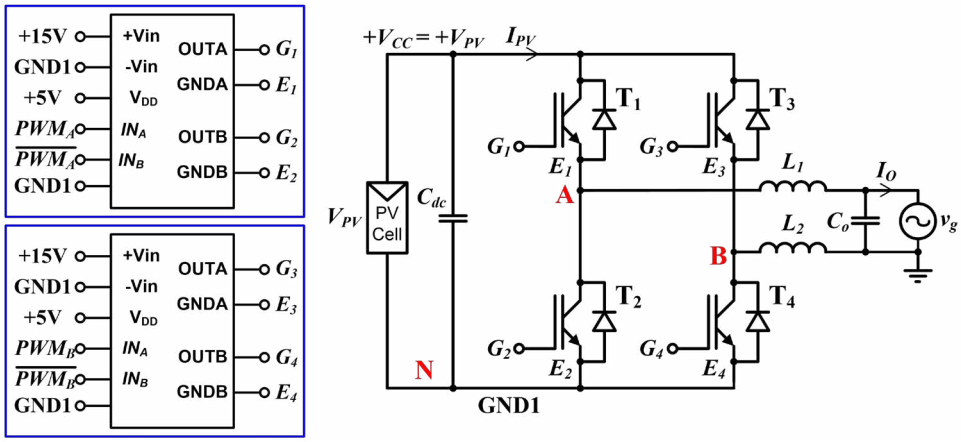


**Figure 5.** Topology of the H4 full bridge inverter

Mode 1: $T_1$ and $T_4$ are turned ON, which is the positive half-period in the active state and all other switches are turned OFF, resulting in: $V_{DM} = V_{AB} = +V_{CC} = +V_{PV}$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{PV} / 2$

Mode 2: High side switches $T_1$ and $T_3$ are turned ON, which is the positive half-period in the freewheeling (Zero) state, and all other switches are turned OFF, resulting in: $V_{DM} = 0$ and $V_{CM} = +V_{CC} = +V_{PV}$

Mode 3: $T_2$ and $T_3$ are turned ON, which is the negative half-period in the active state and all other switches are turned OFF, resulting in: $V_{DM} = -V_{CC} = -V_{PV}$ and $V_{CM} = +V_{CC} / 2 = +V_{PV} / 2$.

Mode 4: Low side switches $T_2$ and $T_4$ are turned ON, which is the negative half-period in the freewheeling (Zero) state, and all other switches turned OFF resulting in: $V_{DM} = 0$ and $V_{CM} = 0$.

The time-domain waveforms of the simulated in SPICE programme control signals, as well the inverter output voltages and currents are shown in Figure 6.

As we see in Figure 6.c, the CM voltage of the H4 full bridge inverter is not constant and it varies during the zero states between +VDC and 0, leading to a high ground leakage current $I_{CpVg}$ of almost 1.1 A RMS value, flowing through the PV system. The standards' requirement for a PV transformer-less inverter is less than 300 mA, hence, a full H4 bridge inverter is not suitable for PV transformer-less application.

By inserting an appropriate delay time on the rising edges of all gate control signals, it is possible to avoid the short-circuiting of the DC-link bus, and approximately achieve zero voltage switching and to prevent shoot-through currents.

Figure 7a shows the time waveforms of the PWM control signals generated in the part of one selected period Tc and the control signals VGE on the input of the IGBTs, generated by drivers assigned to these transistors. Figure 7b shows the simulated time waveforms of the IGBT collector currents $I_{CT1}$, $I_{CT2}$, $I_{CT3}$, $I_{CT1}$ when switching a constant load current $I_O = 25A$ in a selected part of the switching period. On the rising edge of the $PWM_A$ signal, $T_1$ is turned on with the $I_{CT1}$ forward (the body diode conducts), while $T_2$ is turned off with the $I_{CT2}$ reverse. On the falling edge of the $PWM_A$ signal, $T_1$ is turned off with the $I_{CT1}$ reverse, while $T_2$ is turned on with the $I_{CT2}$ forward. As we see in Figure 8b, optimal turn-on delay time of the transistors and significant limitation of the shoot-through currents have been achieved in our project by selecting .

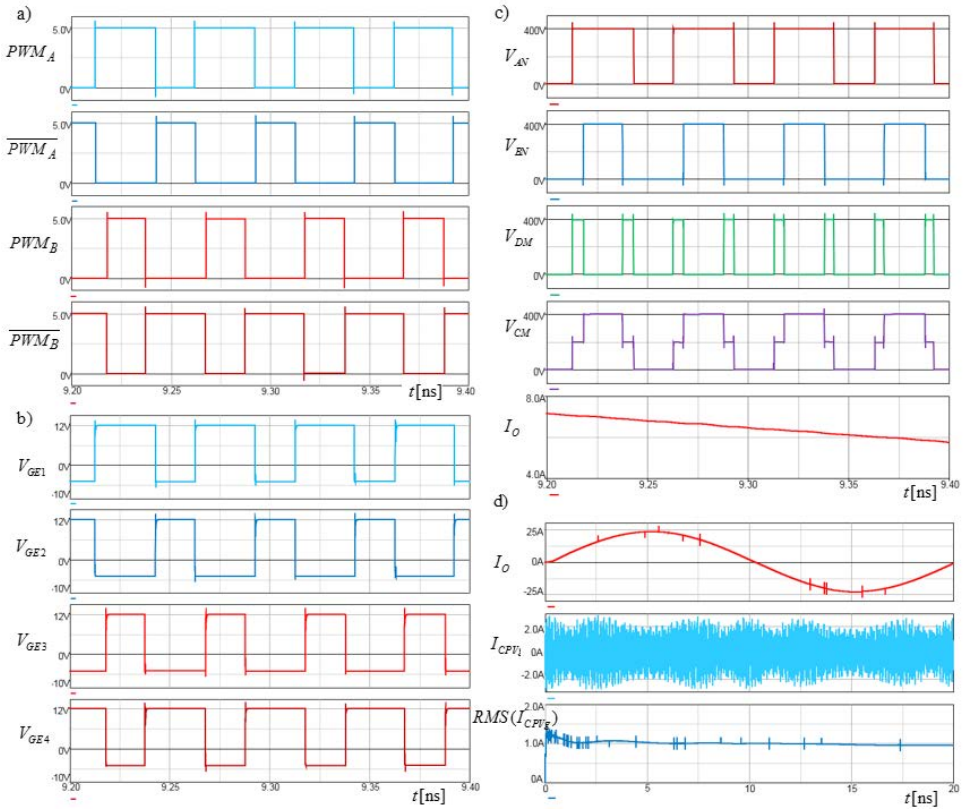


**Figure 6.** PSPICE simulation results of the control signals, as well the H4 inverter output voltages and currents: a) Control signal generated by the extended NBDD PWM modulator in part of the grid voltage period; b) Control signals $V_{GE}$ on the input of the IGBTs, generated by drivers assigned to these transistor; c) $V_{AN}$, $V_{BN}$ voltages at the H4 bridge outputs, Differential Mode $V_{DM}$ voltage and Common Mode $V_{CM}$ voltage at the H4 bridge outputs, d). Load current $I_O$ of the grid-tied inverter, leakage current $I_{CpVg}$ and its RMS value over the full period of the grid voltage

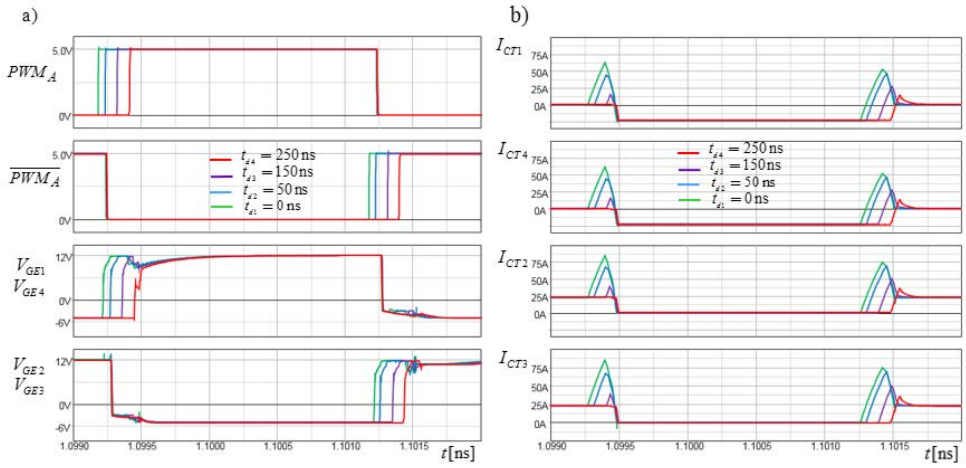


**Figure 7.** Switching constant load current $I_O$ = 25A in a selected part of the switching period: a) Control signals; b) IGBT collector currents $I_{CT1}$, $I_{CT2}$, $I_{CT3}$, $I_{CT1}$

Figure 8 shows the energy efficiency characteristics of the H4 inverter connected to the grid as a function of the output power $P_L$, at the maximum deviation from the rated value of the grid voltage: RMS $V_g$ = 253V. The optimal way of the IGBT transistors switching (when turning off each IGBT, the control voltage at the driver output has a negative value $V_{GE}$ = −5V, quickly discharging the input capacitance $C_{GE}$ of the transistor), as well as the selection of the optimal delay time of switching on each IGBT, result in significant reduction of switching losses and high efficiency of the inverter.

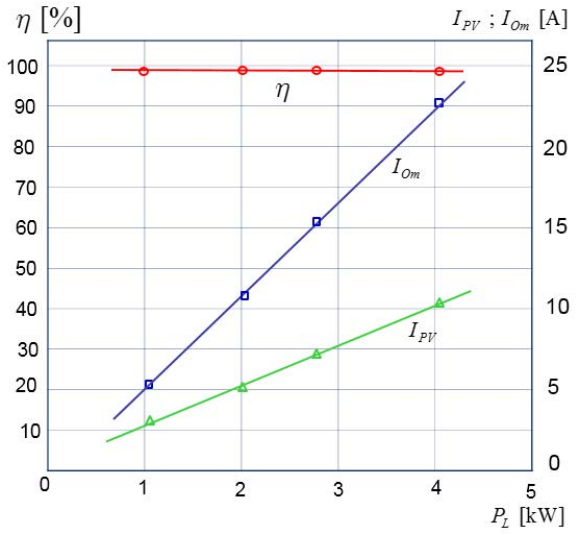


**Figure 8.** Efficiency of the grid-tied H4 inverter vs. output power $P_L$

Equation (1) shows that the frequency spectrum of the NBDD modulation scheme contains no harmonics of the modulating signal, no harmonics of the switching frequency, and no intermodulation components around odd multiples of the switching frequency. Practically, effective sampling frequency for DM voltage at the H-bridge outputs is doubled, without increasing the transition frequency on the output. The output LC low-pass filter, which couples the inverter output with the grid, easily suppresses unwanted components of the PWM output voltage frequency spectrum, limits the output current ripple and reduces EMI. The introduced delay time $t_{d4}$ = 250ns of the turning on the transistors is only 1,25' $10^{-5}$ part of the switching period , and practically has very small effect on the *THD* of the output current.

## 3.2. H5 full bridge inverter

One of the method to minimize the leakage current is an isolation between the input PV source and the output grid source during the zero-state by modifying the PWM in order to keep the CM voltage constant, as in the H5 and H6 topologies [4,5,8,12].

Figure 9 shows the topology of the H5 full bridge inverter, which is driven by the $S_1$, $\bar{S}_1$, $S_2$, $\bar{S}_2$, $S_3$ signals with $F_c$ switching frequency generated by the extended NBDD PWM modulator shown in Figure 2a, or PSC PWM one shown in Figure 3a. The DM output voltage can achieve three level and there are four modes of operation.

Mode 1: $T_5$, $T_1$ and $T_4$ are turned ON, which is the positive half-period in the active state, and all other switches are turned OFF. The current during this mode flows through T5, T1 and T4, resulting in: $V_{DM} = V_{AB} = +V_{CC} = +V_{PV}$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$.

Mode 2: $T_1$ is turned ON, which is the positive half-period in the freewheeling (zero) state, and all other switches are turned OFF. The current during this mode flows through $T_1$, and the anti-paralleled diode of $T_3$, $V_{DM} = V_{AB} = 0$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$ .

Mode 3: $T_2$, $T_3$ and $T_5$ are turned ON, which is the negative half-period in the active state, and all other switches are turned OFF. The current during this mode flows in the opposite direction through $T_2$, $T_3$ and $T_5$, resulting in: $V_{DM} = V_{AB} = -V_{CC} = -V_{PV}$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$.

Mode 4: $T_3$ is turned ON, which is the negative half-period in the freewheeling (zero) state, and all other switches are turned OFF. The current during this mode flows through T3 and the anti-paralleled diode of $T_1$, $V_{DM} = V_{AB} = 0$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$.

The time-domain waveforms of the simulated in SPICE programme the output voltages and currents of the H5 inverter are shown in Figure 10a, while zoomed view of the same time-domain waveforms as in Figure 10a, but presented in the part of one selected period Tc are shown in Figure 10b.

As can be seen in Figure 10, Common Mode $V_{CN}$ voltage at the H bridge output is in practice not constant $V_{PV}/2$, as described above in modes 2 and 4 of operation, but varies over the entire supply voltage range $V_{PV}$, which results also in the inherent leakage current. For example, during the switching DM output voltage from the positive half-period in the active state (Mode 1: $T_5$, $T_1$ and $T_4$ are turned ON, and all other switches are turned OFF) to the freewheeling state (Mode 2: $T_1$ is turned ON, and all other switches are turned OFF – the current during this mode flows through $T_1$, and the anti-paralleled diode of $T_3$), the junction capacitors $C_{S5}$ and $C_{S4}$ are charged, and the junction capacitors $C_{S2}$ and $C_{S3}$ are discharged.

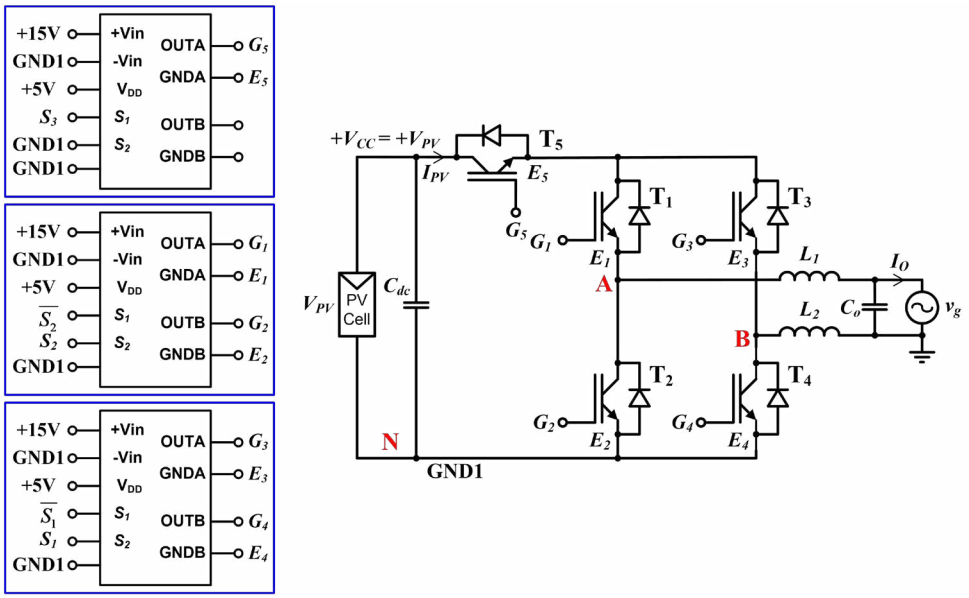


**Figure 9.** Topology of the H5 full bridge inverter

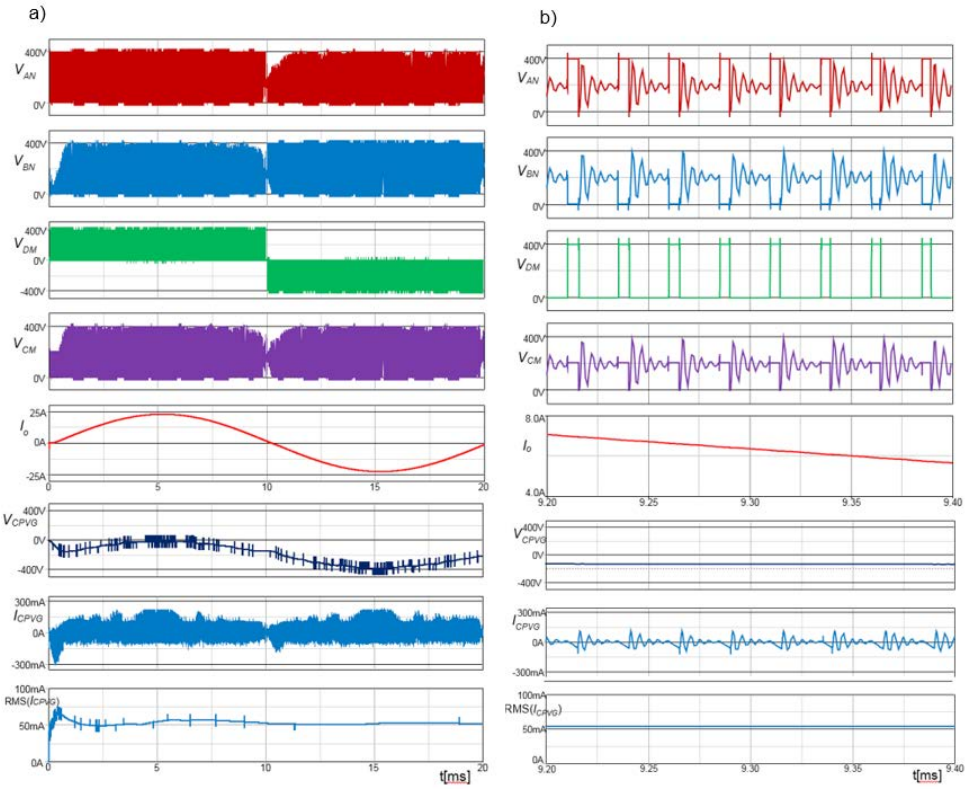


**Figure 10.** PSPICE simulation results of the H5 inverter output voltages and currents (a) and zoomed view of these voltages and currents (b): From top to bottom; $V_{AN}$, $V_{BN}$ voltages at the H5 bridge outputs; $V_{DM}$, $V_{BN}$ Differential Mode $V_{DM}$ voltage and Common Mode $V_{CM}$ voltage at the H5 bridge outputs; load current $I_O$ of the grid-tied inverter; voltage at the $C_{PVg}$ capacitance; instantaneous values of the leakage current $I_{CpVg}$ ;and its RMS value over the full period of the grid voltage

Transient charging and discharging operation of the switch junction capacitors is demonstrated in Figure 11a, whereas the equivalent circuit with the initial voltage on each junction capacitor is shown in Figure 11b.

The terminal voltage $V_{AN}$ increases and the terminal voltage $V_{BN}$ decreases due to the charging and discharging operation. According to Kirchhoff's current law, once the antiparallel diode of switch $T_3$ is conducted, to enter the freewheeling operation stage, the terminal voltages can be derived by [4]:

$$V_{AN} = V_{BN} = \frac{C_{S2} + C_{S5}}{C_{S2} + C_{S5} + C_{S4}} V_{CC} \tag{11}$$

According to equation (11), to receive both terminal voltages VAN and VBN equal Vbus/2, junction capacitors should meet the condition:

$$C_{S4} = C_{S2} + C_{S5} \tag{12}$$

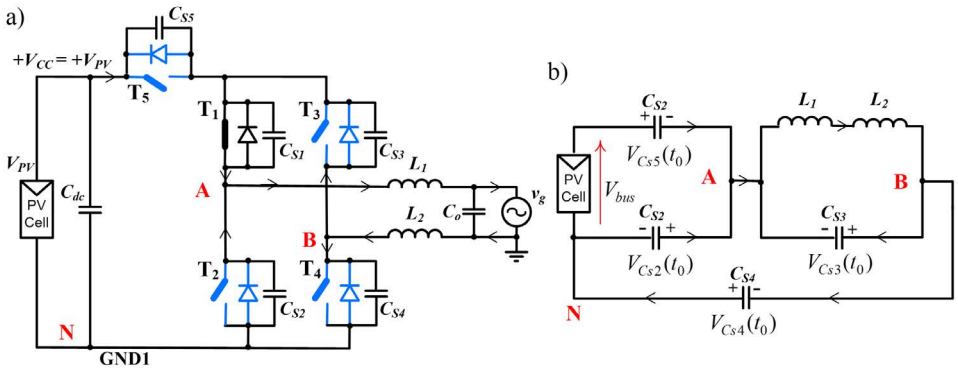


**Figure 11.** Transient charging and discharging operation of the switch junction capacitors: a) Transient operation; b) Equivalent circuit

Practically, condition (12) is not fulfilled, therefore the total high-frequency CM voltage $V_{CM}$ is not kept constant and by parasitic capacitance $C_{PVg}$ flows unexpected leakage current. Furthermore, during the freewheeling stage, when $T_1$, $T_3$ are turned ON, and all other switches are turned OFF, the terminals A and B are floating, and an additional resonant path is formed, which is shown in Figure 12.

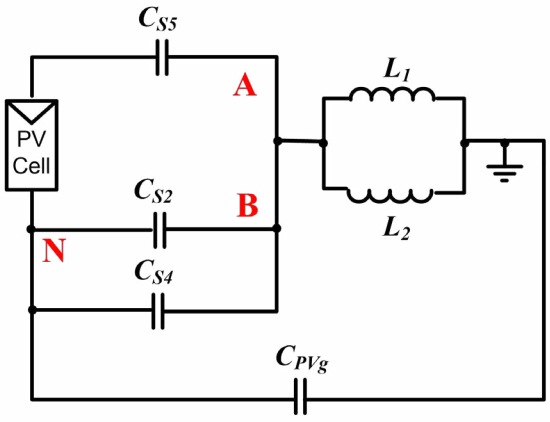


**Figure 12.** Resonant path during freewheeling stage (modes 2 and 4)

In this state, a high-frequency resonant circuit is formed in which leakage currents can also be generated. The resonance frequency can be calculated by [4]:

$$f_r = \frac{1}{2p\sqrt{L_{eq} C_{eq}}} \tag{13}$$

where:

$$L_{eq} = \frac{L_1 L_2}{L_1 + L_2} \quad ; \tag{14}$$

$$C_{eq} = \frac{(C_{S2} + C_{S4} + C_{S5})C_{PVg}}{C_{S2} + C_{S4} + C_{S5} + C_{PVg}} \approx C_{S2} + C_{S4} + C_{S5}$$

## 3.3. AC-based H6 transformerless full bridge inverter

Various topologies have been developed and researched to disconnect the dc and ac sides of the full-bridge inverter in the freewheeling modes for keeping the CM voltage constant [1–6,8,12].

Figure 13 shows the topology of the AC-based H6 transformerless full bridge inverter, which is driven by the $S_1$, $\bar{S}_1$, $S_2$, $\bar{S}_2$ signals with $F_c$ switching frequency, generated by the extended NBDD PWM modulator shown in Figure 2a, or PSC PWM one shown in Figure 3a

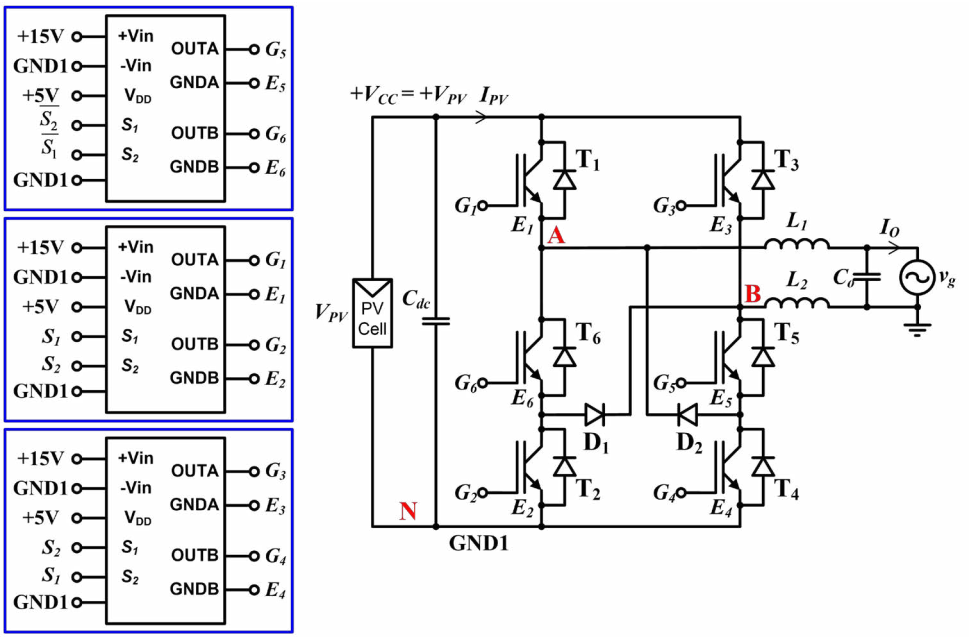


**Figure 13.** Topology of the AC-based H6 transformerless Inverter

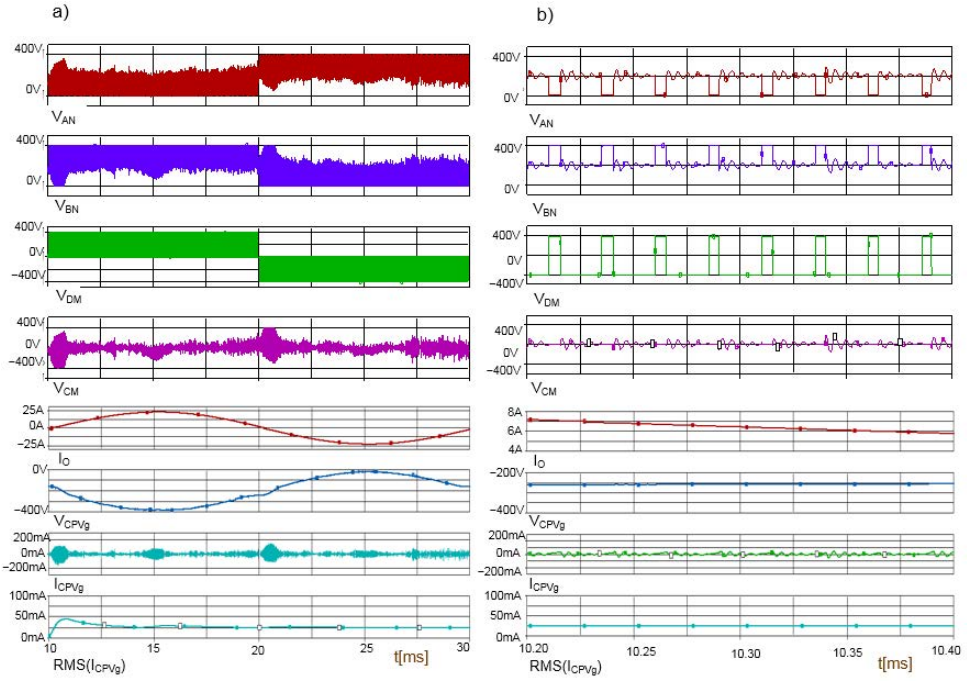


**Figure 14.** PSPICE simulation results of the H6 inverter output voltages and currents (a) and zoomed view of these voltages and currents (b): From top to bottom; $V_{AN}$, $V_{BN}$ voltages at the H6 bridge outputs; Differential Mode $V_{DM}$ voltage and Common Mode $V_{CM}$ voltage at the H6 bridge outputs; load current $I_O$ of the grid-tied inverter; voltage at the $C_{PVg}$ capacitance; instantaneous values of the leakage current $I_{CpVg}$; and its RMS value over the full period of the grid voltage

The DM output voltage can achieve three level and there are four modes of operation.

Mode 1: $T_1$, $T_4$ and $T_5$ are turned ON, which is the positive half-period in the active state, and all other switches are turned OFF. The current during this mode flows through $T_1$, $T_4$ and $T_5$, resulting in: $V_{DM} = V_{AB} = +V_{CC} = +V_{PV}$ and the CM voltage $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$.

Mode 2: $T_5$ is turned ON, which is the positive half-period in the freewheeling (zero) state, and all other switches are turned OFF. The current during this mode flows through $T_5$, and $D_2$. resulting in: $V_{DM} = V_{AB} = 0$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$.

Mode 3: $T_2$, $T_3$ and $T_6$ are turned ON, which is the negative half-period in the active state, and all other switches are turned OFF. The current during this mode flows in the opposite direction through $T_2$, $T_3$ and $T_6$. $V_{DM} = V_{AB} = -V_{CC} = -V_{PV}$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$.

Mode 4: $T_6$ is turned ON, which is the negative half-period in the freewheeling (zero) state, and all other switches are turned OFF. The current during this mode flows through $T_6$ and $D_1$. The same as in mode 2: $V_{DM} = V_{AB} = 0$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$.

The time-domain waveforms of the simulated in SPICE programme the output voltages and currents of the H6 inverter are shown in Figure 14a, while zoomed view of the same time-domain waveforms, but presented in the part of one selected period $T_c$ are shown in Figure 14b.

Similarly to H5 and H6 inverters, switching of the junction capacitances of the IGBTs causes the total high-frequency CM voltage $V_{CM}$ not to be held constant, and some leakage current flows through the parasitic capacitance $C_{PVg}$.

## 3.4. AC-based HERIC transformerless full bridge inverter

Figure 15 shows the topology of the AC-based HERIC transformerless full bridge inverter, containing a bidirectional switch inserted between the terminal A and terminal B [1–6]. This bidirectional switch can be implemented by full-bridge diode module plus one IGBT (Figure 15a), two parallel-connected reverse blocking IGBTs (IGBT connected in series with the diode) (Figure 15b) or by two anti-series-connected IGBTs (Figure 15c) [4]. In the circuits shown in Figure 15, Schottky diodes STPSC20065D were used. The IGBTs are driven by the $S_1$, $S_2$ and $S_3$ signals with $F_c$ switching frequency, generated by the extended NBDD PWM modulator (Figure 2a), or PSC PWM one (Figure 3a). When the bidirectional switch is in the turn-ON state, the zero voltage level is generated, which is completely decoupled with the PV panels. This results in constant CM voltage.

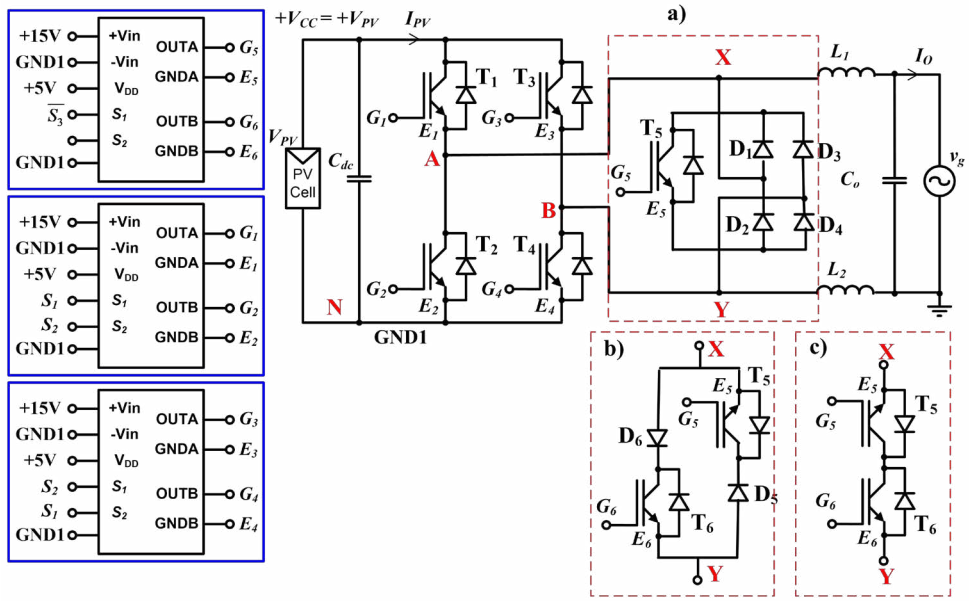


**Figure 15.** Topology of the AC-based HERIC transformerless inverter. Implementation of the bidirectional switch in the form: a) Full-bridge diode module plus one IGBT; b) Two parallel-connected reverse blocking IGBTs; c) Two anti-series-connected IGBTs.

The DM output voltage can achieve three level and there are four modes of operation.

Mode 1: $T_1$ and $T_4$ are turned ON, which is the positive half-period in the active state, and all other switches are turned OFF. The current during this mode flows through $T_1$ and $T_4$, resulting in: $V_{DM} = V_{AB} = +V_{CC} = +V_{PV}$ and the CM voltage $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$.

Mode 2: $T_5$ and $T_6$ are turned ON, which is the positive half-period in the freewheeling (zero) state, and all other switches are turned OFF. The current during this mode flows through $T_5$, and antiparallel diode $D_6$. resulting in: $V_{DM} = V_{AB} = 0$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$ .

Mode 3: $T_2$ and $T_3$ are turned ON, which is the negative half-period in the active state, and all other switches are turned OFF. The current during this mode flows in the opposite direction through $T_2$ and $T_3$, $V_{DM} = V_{AB} = -V_{CC} = -V_{PV}$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$

Mode 4: $T_5$ and $T_6$ are turned ON, which is the negative half-period in the freewheeling (zero) state, and all other switches are turned OFF. The current during this mode flows through $T_6$ and antiparallel $D_5$. In this Mode: $V_{DM} = V_{AB} = 0$ and $V_{CM} = (V_{AN} + V_{BN}) / 2 = +V_{CC} / 2 = +V_{PV} / 2$ .

The time-domain waveforms of the simulated in SPICE programme the output voltages and currents of the HERIC inverter are shown in Figure 16a, while zoomed view of the same time-domain waveforms, but presented in the part of one selected period $T_c$ are shown in Figure 16b.

The AC-based HERIC transformerless inverter contains only two switches in conduction state at any operation mode, which can reduce the conduction losses compared with the dc-based decoupling inverters. To implement fast, bidirectional switches between terminals A and B, silicon carbide Schottky power diodes should be used in these circuits.

Similarly to H5, switching of the junction capacitances of the IGBTs causes the total high-frequency CM voltage $V_{CM}$ not to be held constant, and some leakage current flows through the parasitic capacitance $C_{PVg}$.

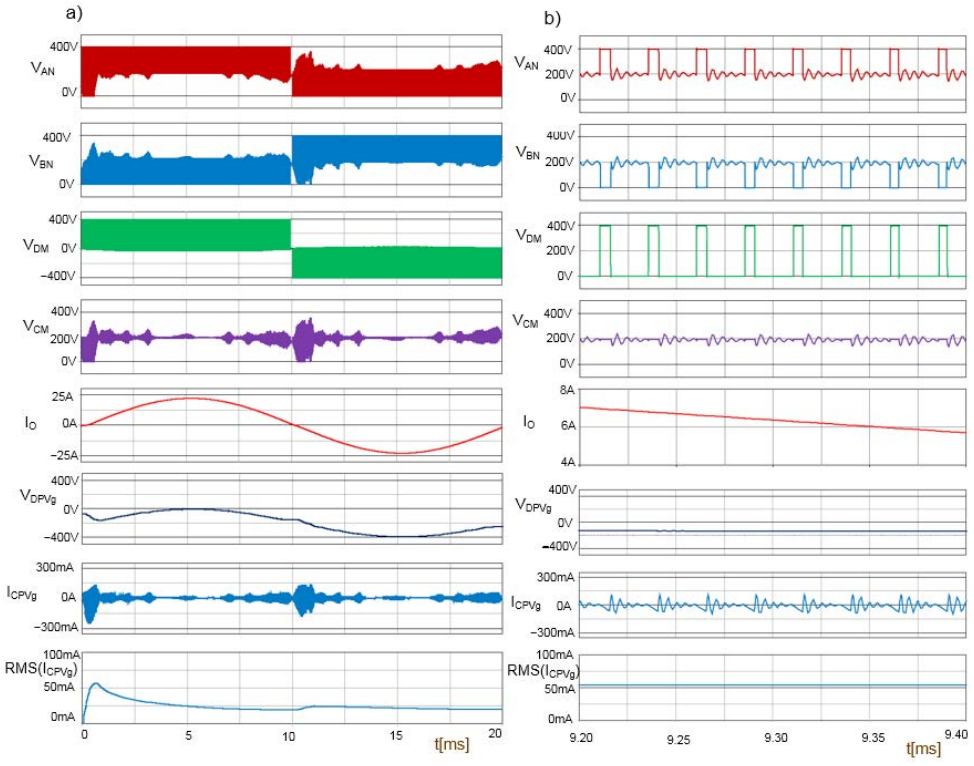


**Figure 16.** PSPICE simulation results of the HERIC inverter output voltages and currents (a) and zoomed view of these voltages and currents (b): From top to bottom; $V_{AN}$, $V_{BN}$ voltages at the HERIC bridge outputs; Differential Mode $V_{DM}$ voltage and Common Mode $V_{CM}$ voltage at the HERIC bridge outputs; load current $I_O$ of the grid-tied inverter; voltage at the $C_{PVg}$ capacitance; instantaneous values of the leakage current $I_{CPVg}$; and its RMS value over the full period of the grid voltage

## 3.5. Derived HERIC inverter — clamping topology

An isolation between the input PV source and the output grid source during the zero-state, to minimize the leakage current, forms the group of dc-based decoupling transformerless inverters (H5, H6 inverters and their derivations). When a bidirectional switch is inserted between the terminal A and terminal B, the group of ac-based decoupling transformerless Inverters is formed (HERIC inveertr and its derivations). However, H5, H6 and HERIC inverters discussed earlier do not contain the clamping ability to avoid the floating operation.

Figure 17 presents a family of derived HERIC-based clamping topologies. with leakage current elimination. In order to effectively clamp the common-mode voltage as a constant value and avoid the floating operation, the passive (Figures 17a, 17b) or active (Figure 17c) clamping circuits can be applied.

In the circuits shown in Figure 17, Schottky diodes STPSC20065D were used. HERIC-based clamping inverter is controlled identically as HERIC inverter in Figure 15. By turning on the clamping and bidirectional switches, the common-mode voltage is clamped to half of the bus voltage, which can completely eliminate the additional leakage current.

The time-domain waveforms of the simulated in SPICE the output voltages and currents of the HERIC-based clamping inverter are shown in Figure 18a, while zoomed view of the same time-domain waveforms, but presented in the part of one selected period Tc are shown in Figure 18b.

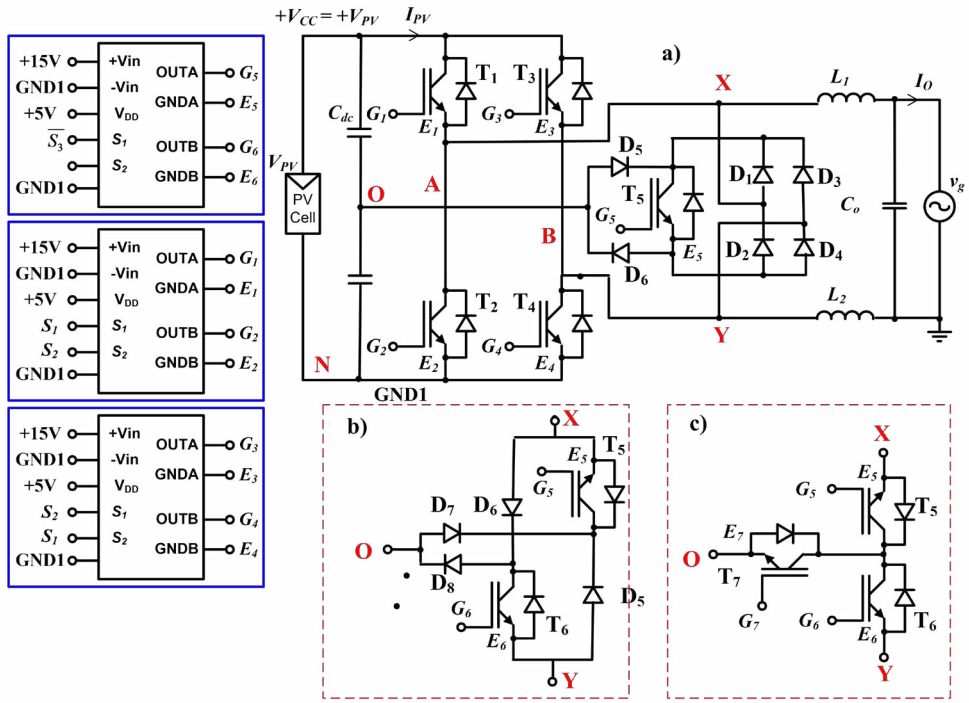


**Figure 17.** Derived HERIC-based clamping topologies. a), b) Passive clamping topology; c) Active clamping topology

## 4. Comparison of the tested H4, H5, H6 and HERIC inverters

Depending of the accuracy of the used models of elements and components, simulations of tested inverters taking into account generation of PWM signals at the output of the extended PSCPWM modulator, transmission of control signals to the output of the IGBT gate drivers with galvanic isolation and switching of the power IGBT transistors in the circuit of the tested inverter reflect the inverter operation and properties in reality, based on its description with the help of computational models. These simulations require very long execution time, however allow to evaluate the performance of the reviewed inverters under different load conditions.

Table 1 shows the energy efficiency and RMS value of leakage current of the tested H4, H5, H6 and HERIC

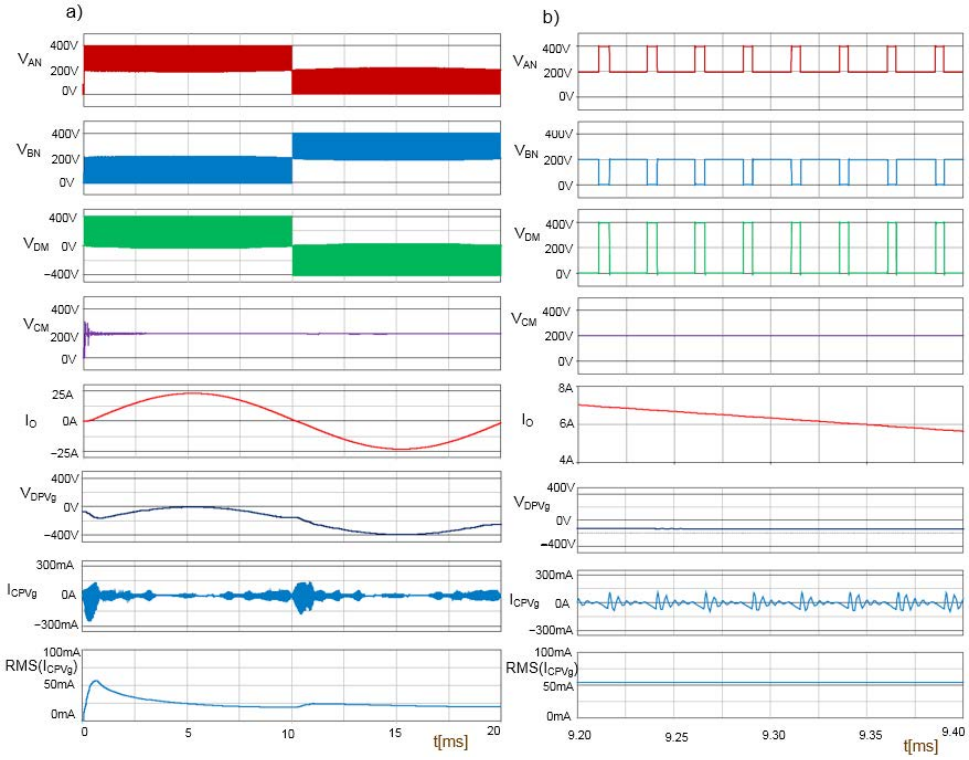


**Figure 18.** PSPICE simulation results of the inverter output voltages and currents of the HERIC-based clamping topology (a) and zoomed view of these voltages and currents (b): From top to bottom; $V_{AN}$, $V_{BN}$ voltages at the HERIC bridge outputs; Differential Mode $V_{DM}$ voltage and Common Mode $V_{CM}$ voltage at the HERIC bridge outputs; load current $I_O$ of the grid-tied inverter; voltage at the $C_{PVg}$ capacitance; instantaneous values of the leakage current $I_{CPVg}$; and its RMS value over the full period of the grid voltage.

inverters. All tested inverters have high energy efficiency from ~97.5% to ~98.8%, depending on the power at the output of the inverter in the range from ~1kW to ~4.2kW. High energy efficiency of all tested inverters across the power output range indicates that IGBTs are optimally controlled to minimize both conductive power losses and switching power losses of IGBT transistors. It was achieved by selecting optimal turn-on delay time $t_{d4}$ = 250ns of all IGBTs, resulting in a significant reduction of shoot-through currents when switching transistors, as well as providing a fairly high driving voltage $V_{GS}$ = 12V in the turn-on state of the IGBTs.

**Table 1.** Efficiency comparison of H4, H5, H6 and HERIC inverters

| $P_L$[W] | 4.19 | 2.76 | 2.08 | 1.04 | Leakage current RMS ($I_{PVg}$ [mA]) |
|---|---|---|---|---|---|
| $h$[%] of H4 | 98.7 | 98.79 | 98.56 | 97.94 | 1100 |
| $h$[%] of H5 | 97.66 | 97.79 | 97.38 | 97.93 | 50 |
| $h$[%] of H6 | 97.56 | 97.67 | 97.23 | 97.63 | 25 |
| $h$[%] of HERIC | 97.69 | 98.69 | 98.51 | 98.02 | 26 |
| $h$[%] of HERIC – clamping topology | 97.69 | 98.67 | 98.48 | 98.11 | 23 |

The efficiencies of H4 and H6 inverters are slightly higher than H5 and H6 inverters, because H4 and H6 inverters contains only two switches in conduction state at any operation mode, while H5 and H6 inverters contain three switches, resulting in slightly higher conduction losses.

Although H4 inverter has good efficiency characteristic, as well as effective sampling frequency of the DM output signal is doubled without increasing the transition frequency on the output and all harmonics around odd multiples of the switching frequency are eliminated, however its CM output voltage is present at full scale even at very low level of modulating signal, which leads to high unacceptable leakage current. As you can see in Table 1, the RMS of the leakage current is equal to $I_{PVg}$ = 1.1A, significantly exceeding the allowable value of 300 mA. To reduce it to the acceptable level, CM filter must be applied at the output of the inverter, which also increases its cost.

Other tested inverters have low leakage currents, with the lowest value of 23 mA having HERIC-based clamping topology. For all tested inverters, the RMS values of the leakage currents have been calculated for full period $T_m$ = 20ms of the modulating signal, i. e. the power grid voltage period.

Although CM voltages are almost constant at the outputs of these inverters, small leakage currents are generated as a result of overcharging of the IGBT junction capacitances during their switching from the freewheeling state to the active state of positive or negative half-period in created resonant path shown in Figure 12.

## 5. Conclusions

The paper presents analyses and simulations in the SPICE program of leakage currents and energy efficiency under different load conditions of known single-phase transformerless inverters H4, H5, H6 and HERIC.

Based on these analyses and simulations, we can conclude that the leakage current of all single-phase transformerless inverters in the full bridge configuration consists of two components:

1. Leakage current generated at inverter output because the CM voltage are not kept constant in all operating modes.
2. Leakage current generated in the created resonant path during overcharging of the IGBT junction capacitances during their switching from the freewheeling state to the active state of positive or negative half-period.

At the output of the H4 inverter, a CM voltage is generated over the full VCC supply voltage range even at a very low level of modulating signal, which leads to a very high unacceptable level of leakage current. However, the very good frequency characteristics with twice lower switching frequency compared to other inverters may be encouraging for the practical use of the H4 inverter. In this case, a properly designed CM filter with choke inductor must be used at the output of the H4 inverter.

At the outputs of other inverters H5, H6, HERIC is maintained almost constant CM voltage (on the H5 inverter output there are some minor fluctuations), which indicates that very small leakage current is generated in the created resonant path during overcharging of the IGBT junction capacitances. This leakage current depends on the switching frequency, the IGBT junction capacitances and the inductances of the output filter, but approximately does not depend on the parasitic capacitance between the PV panels and ground. When it is necessary to limit the resonant leakage current, it would be necessary to increase the inductances of the output LC filter. However, this would entail a significant increase in the dimensions and costs of the power chokes with a ferrite cores providing high saturation current, and filtering the switching frequency components of the output current.

Simulations of tested inverters taking into account generation of PWM signals at the output of the extended PSCPWM modulator, transmission of control signals to the output of the IGBT gate drivers with galvanic isolation and switching of the power IGBT transistors in the circuit of the tested inverter reflect the inverter operation and properties in reality, based on its description with the help of computational models.

SPICE simulations of the complete inverter circuit including both control and power output circuits have enabled optimisation of system parameters and visualization of results calculations of the entire design process of the inverter, and thus made they much easier to proceed to the practical implementation of the inverter.

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